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EXAMINER	
RUTZ, JARED IAN	
ART UNIT	PAPER NUMBER
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/802,914	FUNAHASHI ET AL.
	Examiner	Art Unit
	Jared I. Rutz	2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4 and 6-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4 and 6-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2-4 and 6-27 as amended on 12/18/2006, are pending in the instant application. Applicant's arguments submitted 12/18/2006 have been carefully and fully considered, but are considered moot in view of the new grounds of rejection presented herein. The new grounds of rejection are necessitated by amendment to the claims, and accordingly, this Office action is made **FINAL**.

Specification

2. The amendments to the specification and the abstract are accepted by the Examiner, and the objection to the Specification presented in the Office action of 9/19/2006 is withdrawn.

Claim Objections

3. **Claims 6 and 13** are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 23, from which claim 6 depends, recites the address conversion unit recited in claims 6 and 13.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 2-4 and 6-27** are rejected under 35 U.S.C. 102(e) as being anticipated by Lasserre et al. (US 6,760,829).

6. **Claim 20** is taught by Lasserre as:

a. *A processor connected to a memory via a data bus, the data bus having a data width, said processor being a second-endian type processor which is usable with a first-endian type processor.* Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Column 9 4-17 shows that the data bus between the processors and memory is 32 bits.

b. *Said processor comprising: a processor bus logically connected to the data bus in a first-endian byte order.* Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

c. *And an address conversion unit operable to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus.* Column 10 line 59 through column 11 line4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

d. *And output the converted address to the memory, when the processor performs a memory access for data having a smaller width than the width of the data bus.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus.

e. *And operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus.* Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request.

7. **Claim 2** is taught by Lasserre as:

f. *The processor according to Claim 20, further comprising a cache memory logically connected to the data bus in a second-endian byte order.* Figure 2B shows L2 Cache 114 connected to L2 traffic control 110. Column 3 lines 52-54 shows that the DSP as shown in figure 2 is connected to the traffic controller via

L2 interface 210, which includes TLB 212. Column 8 lines 42-50 shows that each TLB entry contains information about the endianism of the memory address region represented by the TLB entry. Accordingly, the data stored in the L2 memory, shown at column 3 lines 10-14 to include cache 114, can be stored in either little or big endian format. When data in the second-endian byte order is being accessed, cache 114 is logically connected to traffic control 110 in a second-endian byte order.

g. *Wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.* Column lines 4-17 show that accesses can be made to memory in the same bit-width of the data bus.

8. **Claim 3** is taught by Lasserre as:

h. *The processor according to Claim 20, executing a program that defines structure data which includes data that is smaller than a basic word length.* Page 5 lines 13-15 of the specification of the instant application states "*Here, the processor (first processor) may be structured to execute a program that defines structure data which includes data that is smaller than a basic word length...*" Column 9 lines 22-25 shows that a 16 bit value can be written to location 2 of 32 bit memory word 410 of figure 4. As a processor can only access data under the control of a program, it is inherent that the 16 bit value, smaller than the 32 bit word size, is accessed by a program executing on the processor.

i. *Said structure data being shared between said processor and a first-endian type processor via the memory.* Column 8 lines 63-65 show that DSP 400 and CPU 402 can both access memory location 410.

j. *Said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data in a program to be executed by the first-endian type processor.* As shown in figure 4 and discussed in column 9 lines 22-25, location 2 corresponds to bits [15:0] of DSP 400 and bits [31:16] of CPU 402.

9. **Claim 4** is taught by Lasserre as:

k. *The processor according to Claim 3, further comprising a cache memory logically connected to the data bus in a second-endian byte order.* Figure 2B shows L2 Cache 114 connected to L2 traffic control 110. Column 3 lines 52-54 shows that the DSP as shown in figure 2 is connected to the traffic controller via L2 interface 210, which includes TLB 212. Column 8 lines 42-50 shows that each TLB entry contains information about the endianism of the memory address region represented by the TLB entry. Accordingly, the data stored in the L2 memory, shown at column 3 lines 10-14 to include cache 114, can be stored in either little or big endian format. When data in the second-endian byte order is being accessed, cache 114 is logically connected to traffic control 110 in a second-endian byte order.

l. *Wherein the processor reads data from the memory through the cache memory in data units of the same width as the data bus.* Column lines 4-17 show that accesses can be made to memory in the same bit-width of the data bus.

10. **Claim 23** is taught by Lasserre as:

m. *A data sharing apparatus comprising: a data bus having a data width.* Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Column 9 4-17 shows that the data bus between the processors and memory is 32 bits.

n. *A memory.* Figure 4 shows a memory storing memory location 410.

o. *A first-endian processor logically connected to said memory in a first-endian byte order via said data bus.* CPU 402.

p. *A second-endian processor logically connected to said memory in the first-endian byte order via said data bus.* DSP 400. Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

q. *And an address conversion unit operable to perform an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus.* Column 10 line 59 through column 11 line4 shows that memory controller circuitry 706 inverts the least significant address

bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

r. *And output the converted address to the memory, when the second-endian processor performs a memory access for data having a smaller width than the width of the data bus.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus.

s. *And operable to not perform the address conversion when the processor performs a memory access for data having the width of the data bus.* Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request.

11. **Claim 6** is taught by Lasserre as:

t. *The data sharing apparatus according to Claim 23, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus.* Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

u. *And output the converted address to the memory, when the second-endian processor performs a memory access for the data with a smaller width*

than the width of the data bus. Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus.

v. *And operable to not convert any address when the processor performs a memory access for data having the width of the data bus.* Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request.

12. **Claim 7** is taught by Lasserre as:

w. *The data sharing apparatus according to Claim 6, further comprising a transfer unit operable to control data transfer by direct memory access.* Figure 5 shows resources 540, which include a DMA engine. Column 10 lines 28-41 discuss the steps taken when an endianism mismatch is detected.

x. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.* As shown in column 10 lines 34-41, when an endianism mismatch occurs, the abort handler invokes a software routine that converts the data to an alternative endian format.

13. **Claim 8** is taught by Lasserre as:

y. *The data sharing apparatus according to Claim 7, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus.* Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

z. *And output the converted address to the memory.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

aa. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.* Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

14. **Claim 9** is taught by Lasserre as:

bb. *The data sharing apparatus according to Claim 6, wherein the memory stores structure data to be accessed by the first-endian processor and the second-endian processor.* Column 9 lines 22-25 shows that a 16 bit value can be written to location 2 of 32 bit memory word 410 of figure 4.

cc. *The first-endian processor executes a first program that defines the structure data.* Column 9 lines 22-25 shows that when a processor in little-endian mode, CPU 402, writes a 16 bit value to location 2 of memory word 410, it will overwrite 0xDDCC, corresponding to lines [31:16] of the memory bus.

dd. *And the second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.* Column 9 lines 22-25 shows that when a processor in bit-endian mode, DSP 400, writes a 16 bit value to location 2 of memory word 410, it will overwrite 0xBBAA, corresponding to lines [15:0] of the memory bus. To ensure accesses to data objects smaller than the size of the data bus are properly aligned, as discussed at column 9 lines 25-33, memory controller circuitry 706 as discussed at column 10 lines 59 through column 11 line 4 inverts lower order address bits when accesses smaller than a word are made into a memory region storing data in corresponding to a different endianness than the requesting resource.

15. **Claim 10** is taught by Lasserre as:

ee. *The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access.* Resources 540 of figure 5, as discussed at column 9 lines 34-41, include DMA engine 106. Column 10 lines 3-4 shows that resource 700 of figure 7 is

representative of one or more or resources 540 or 550, and therefore is representative of DMA 106.

ff. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.* Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706, responsive to size signals 708, inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

16. **Claim 11** is taught by Lasserre as:

gg. *The data sharing apparatus according to Claim 10, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus.* Column 10 lines 44-45 shows that resource 700 is representative of one or more resources 540 or 550, which includes the DMA engine. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

hh. *And output the converted address to the memory.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

ii. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred*. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

17. **Claim 12** is taught by Lasserre as:

jj. *The data sharing apparatus according to Claim 23, further comprising a cache memory logically connected to the data bus in a second-endian byte order.* Figure 2B shows L2 Cache 114 connected to L2 traffic control 110. Column 3 lines 52-54 shows that the DSP as shown in figure 2 is connected to the traffic controller via L2 interface 210, which includes TLB 212. Column 8 lines 42-50 shows that each TLB entry contains information about the endianism of the memory address region represented by the TLB entry. Accordingly, the data stored in the L2 memory, shown at column 3 lines 10-14 to include cache 114, can be stored in either little or big endian format. When data in the second-endian byte order is being accessed, cache 114 is logically connected to traffic control 110 in a second-endian byte order.

18. **Claim 13** is taught by Lasserre as:

kk. *The data sharing apparatus according to Claim 12, further comprising an address conversion unit operable to convert at least one lower bit of an address so as to indicate a reversed position of data in the data bus.* Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

ll. *And output the converted address to the memory, when the second processor performs a memory access for the data with a smaller width than the width of the data bus.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus.

19. **Claim 14** is taught by Lasserre as:

mm. *The data sharing apparatus according to Claim 13, further comprising a transfer unit operable to control data transfer by direct memory access.* Figure 5 shows resources 540, which include a DMA engine. Column 10 lines 28-41 discuss the steps taken when an endianism mismatch is detected.

nn. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.* As shown in column 10 lines 34-

41, when an endianism mismatch occurs, the abort handler invokes a software routine that converts the data to an alternative endian format.

20. **Claim 15** is taught by Lasserre as:

oo. *The data sharing apparatus according to Claim 14, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus.* Column 10 lines 44-45 shows that resource 700 is representative of one or more resources 540 or 550, which includes the DMA engine. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

pp. *And output the converted address to the memory.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

qq. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.* Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

21. **Claim 16** is taught by Lasserre as:

rr. *The data sharing apparatus according to Claim 13 wherein the memory stores structure data to be accessed by the first-endian processor and the second-endian processor.* Column 9 lines 22-25 shows that a 16 bit value can be written to location 2 of 32 bit memory word 410 of figure 4.

ss. *The first-endian processor executes a first program that defines the structure data.* As a processor can only access data under the control of a program, it is inherent that the 16 bit value, smaller than the 32 bit word size, is accessed by a program executing on the processor. Column 9 lines 22-25 show that the memory access can be performed by either the big endian or little endian processor.

tt. *And the second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program.* Column 9 lines 22-25 show that the memory access can be performed by either the big endian or little endian processor.

22. **Claim 17** is taught by Lasserre as:

uu. *The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access.* Figure 5

shows resources 540, which include a DMA engine. Column 10 lines 28-41 discuss the steps taken when an endianism mismatch is detected.

vv. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination.* As shown in column 10 lines 34-41, when an endianism mismatch occurs, the abort handler invokes a software routine that converts the data to an alternative endian format.

23. **Claim 18** is taught by Lasserre as:

ww. *The data sharing apparatus according to Claim 17, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus.* Column 10 lines 44-45 shows that resource 700 is representative of one or more resources 540 or 550, which includes the DMA engine. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

xx. *And output the converted address to the memory.* Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

yy. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred.* Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

24. **Claim 19** is taught by Lasserre as:

zz. *A method of sharing data in a data processing apparatus which includes a first-endian type processor and a second-endian type processor, and a memory to which both processors are connected via a data bus in a first-endian byte order.* Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

aaa. *The method comprising: causing the second processor to execute a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared in the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data for the first-endian type*

processor. Column 9 lines 18-25 shows that the processors of different endianness can access data objects smaller than a word, and that because the different processors have different endianness, the order of the byte addresses is reversed, as shown in figure 4.

bbb. *And performing an address conversion on at least one lower bit of an address so as to indicate a reversed position of data in the data bus, in the case where the second-endian processor performs a memory access for data with a smaller width than the width of the data bus, and not performing the address conversion in the case where the second-endian processor performs a memory access for data having the width of the data bus.* As discussed at column 9 lines 18-33, when a processor accesses a data object smaller than the width of the 32 bit word, if the endianness of the processor differs from the endianness used to store the data in the memory, the data object must be offset by conditionally complementing byte enables based on the endianness mode. As discussed at column 10 line 59 through column 11 line 4, when an access request is made to a memory region having different endianness than the requesting resource, memory controller circuitry 706 adjusts address bits by inverting selected bits according to data size signals 708 to reverse the address ascension order to agree with the endianism of the selected memory region.

25. **Claims 21, 24, and 26** are taught by Lasserre as:

ccc. *Wherein the first-endian type is big-endian and the second-endian type is little-endian*. Column 10 lines 42-63 shows that each resource 700, which includes resources 540 or 550, which is shown at column 9 lines 40-46 to include DMA engine 106, coprocessors 108, and processors 102 and 104, contains an endianism-ID circuitry 712 and memory controller 706. The addresses are adjusted when the endianism of resource 700, indicated by endianism-ID circuitry 712, does not match the endianism of the memory region being accessed, indicated by endianism attribute signal 710. Accordingly, when the processor is little-endian, the second-endian type, such as CPU 402 of figure 4, and performs a sub-word memory access to a region of memory that stored data in a big-endian format as indicated by endianism attribute signal 710, the processing recited in claims 21, 24, and 26 is performed.

26. **Claim, 22, 25, and 27** are taught by Lasserre as:

ddd. *The processor according to claim 20, wherein the first-endian type is little-endian and the second-endian type is big-endian*. Column 10 lines 42-63 shows that each resource 700, which includes resources 540 or 550, which is shown at column 9 lines 40-46 to include DMA engine 106, coprocessors 108, and processors 102 and 104, contains an endianism-ID circuitry 712 and memory controller 706. The addresses are adjusted when the endianism of resource 700, indicated by endianism-ID circuitry 712, does not match the endianism of the memory region being accessed, indicated by endianism attribute signal 710.

Accordingly, when the processor is big-endian, the second-endian type, such as DSP 400 of figure 4, and performs a sub-word memory access to a region of memory that stored data in a little-endian format as indicated by endianism attribute signal 710, the processing recited in claims 21, 24, and 26 is performed.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

28. Qureshi et al. (US 2004/0030856) teaches a method and apparatus wherein a processor of a first endian type accesses a memory storing data in a second endian type, wherein least significant bits of the address are inverted for a sub-word access, see paragraph 20.

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian R. Peugh
Primary Examiner
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